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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,789	03/16/2004	Andy Yu	20359.3	3122

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,789	YU ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15-17 and 41-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15-17 and 41-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed February 22, 2006 has been entered. Claims 12-14, 18-26, 39 and 40 have been cancelled. Claims 1, 6 and 10 have been amended. Claims 41-68 have been added. Claims and 1-11, 15-17 and 41-68 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 15-17 and 41-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong (U.S. Patent No. 5,427,968) in view of Sung (U.S. Patent No. 6,018,178) of record.

With respect to claim 1, Hong teaches an electrically alterable memory device substantially as claimed including:

a second semiconductor layer (50), doped with a second dopant (P), the second semiconductor layer (50) having a top side;

two spaced-apart diffusion regions (62) embedded in the top side of the semiconductor layer (50), each diffusion region (62) doped with the first dopant (N) in a second concentration, the two diffusion regions (62) including a first diffusion region (62) and a second diffusion region (62), and a first channel region defined between the first diffusion region (62) and the second diffusion region (62);

a first floating gate (60) having a first height and comprised of a conductive material, the first floating gate (60) disposed adjacent the first diffusion region (62) and above the first channel region and separated therefrom by a first insulator region (58), the first floating gate capable of storing electrical charge;

a second floating gate (60) having a second height and comprised of a conductive material, the second floating gate (60) disposed adjacent the second diffusion region (62) and above the first channel region and separated therefrom by a second insulator region (58), the second floating gate (60) capable of storing electrical charge; and

a control gate (66) having a third height that higher than the first height and the second height and comprised of a conductive material, the control gate (66) disposed laterally between the first floating gate (60) and the second floating gate (60), the control gate (66) separated from the first floating gate (60) by a first vertical insulator layer (64) and separated from the second floating gate (60) by a second vertical insulator layer (64), the control gate acting as a word select line, the control gate (66) further being above the first channel region without overlapping the two spaced-apart diffusion regions (62) and separated therefrom by a third insulator region (54). (See Fig. 4d).

Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.

However, Sung teaches an electrically alterable memory device formed on a semiconductor substrate (1) having a first semiconductor layer (2) doped with a first dopant (N)

in a first concentration that is smaller than that of the diffusion region (14) and a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant (P), that has an opposite electrical characteristic than the first dopant (N), the second semiconductor layer (3) having a top side. (See Figs. 1 and 9).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.

With respect to claim 41, Hong teaches an electrically alterable memory device substantially as claimed including:

a second semiconductor layer (50), doped with a second dopant (P), the second semiconductor layer (50) having a top side;

two spaced-apart diffusion regions (62) embedded in the top side of the second semiconductor layer (50), each diffusion region (62) doped with the first dopant (N) in a second concentration, the two diffusion regions (62) including a first diffusion region (62) and a second diffusion region (62), and a first channel region defined between the first and second diffusion region (62);

a first floating gate (60) having a left side and a right side and comprising of a conductive material, the first floating gate (60) disposed adjacent the first diffusion region (62) and above the first channel region and separated therefrom by a first insulator region (58), the first floating gate (62) capable of storing electrical charge;

a second floating gate (60) having a left side and a right side and comprising of a conductive material, the second floating gate (60) disposed adjacent the second diffusion region (62) and above the first channel region and separated therefrom by a second insulator region (58), the second floating gate (60) capable of storing electrical charge; and

a control gate (66) comprising of a conductive material, the control gate (66) disposed laterally between the first and second floating gate (60), the control gate (66) separated from the first floating gate (60) by a third insulator layer (64) and separated from the second floating gate (60) by a fourth insulator layer (64), the control gate (66) covering the first and second floating gate (60) on at least right side and left side, the control gate (66) further being above the first channel region and separated therefrom by a third insulator region (54). (See Fig. 4d).

Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.

However, Sung teaches an electrically alterable memory device formed on a semiconductor substrate having a first semiconductor layer (2) doped with a first dopant (N) in a first concentration and a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant (P), that has an opposite electrical characteristic than the first dopant (N), the second semiconductor layer (3) having a top side. (See Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor

substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.

With respect to claims 2 and 42, in view of Sung, the first semiconductor layer is doped with first dopant (N-type) and the second semiconductor layer is doped second dopant (P-type), respectively.

Thus, Hong and Sung is shown to teach all the features of the claim with the exception of alternatively doping the first and second semiconductor layers with the opposite type dopants.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to dope the first and second semiconductor layers of Hong, in view of Sung, with any of the opposing dopant type, since it has been held that a mere reversal of the essential working parts, e.g., N-type instead of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

With respect to claims 3 and 43, the first dopant of Hong has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claims 4, 6, 44 and 46, the first and second insulator region (58) of Hong having a thickness that allows tunneling of charge between the first floating gate (60) and the first channel region.

With respect to claims 5, 7, 45 and 47, the thickness of the first and second insulator region (58) of Hong is 100 Å (between 70 Å and 110 Å).

With respect to claims 8-11 and 48-51, the first and second vertical insulator (64) of Hong is made from a silicon dioxide or oxide nitride oxide (ONO) having a thickness that provides capacitance between the first and second floating gate (60) and the control gate (66), respectively, and the first and second vertical insulator (64) preventing leakage between the first and second floating gate (60) and the control gate (66), respectively.

With respect to claims 15 and 52, the first and second floating gate (60) of Hong each inherently being capable of storing multiple levels of charge.

With respect to claims 16 and 53, the first and second floating gate (60) of Hong each inherently being capable of storing four levels of charge.

With respect to claims 17 and 54, an oxide layer (58) of Hong is disposed on top of each diffusion region (62).

3. Claims 55-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong (U.S. Patent No. 5,576,232) in view of Sung '178.

With respect to claim 55, Hong teaches an electrically alterable memory device substantially as claimed including:

a second semiconductor layer (5), doped with a second dopant (P), the second semiconductor layer (5) having a top side;

two spaced-apart diffusion regions (59) embedded in the top side of the semiconductor layer (5), each diffusion region (59) doped with the first dopant (N) in a second concentration,

the two diffusion regions (59) including a first diffusion region (59) and a second diffusion region (59), and a first channel region defined between the first and second diffusion region (59);

a first floating gate (580) having a first height and comprised of a conductive material, the first floating gate (580) disposed adjacent the first diffusion region (59) and above the first channel region and separated therefrom by a first insulator region (57), the first floating gate (580) capable of storing electrical charge;

a second floating gate (580) having a second height and comprised of a conductive material, the second floating gate (580) disposed adjacent the second diffusion region (59) and above the first channel region and separated therefrom by a second insulator region (57), the second floating gate (580) capable of storing electrical charge; and

a control gate (520) having at least two lateral sides and comprises of a conductive material, the control gate (520) disposed laterally between the first and second floating gate (580), the control gate (520) separated from the first floating gate (580) by a first vertical insulator layer (5570) and separated from the second floating gate (580) by a second vertical insulator layer (570), the control gate being covered by the first and second floating gate (580) on more than one lateral side, the control gate being separated from the first channel region by a third insulator region (51). (See Fig. 7h).

Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.

However, Sung teaches an electrically alterable memory device formed on a semiconductor substrate having a first semiconductor layer (2) doped with a first dopant (N) in a first concentration and a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant (P), that has an opposite electrical characteristic than the first dopant (N), the second semiconductor layer (3) having a top side. (See Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.

With respect to claim 56, in view of Sung, the first semiconductor layer is doped with first dopant (N-type) and the second semiconductor layer is doped second dopant (P-type), respectively.

Thus, Hong and Sung are shown to teach all the features of the claim with the exception of alternatively doping the first and second semiconductor layers with the opposite type dopants.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to dope the first and second semiconductor layers of Hong, in view of Sung, with any of the opposing dopant type, since it has been held that a mere reversal of the essential working parts, e.g., N-type instead of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

With respect to claim 57, the first dopant of Hong has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claims 58 and 60, the first and second insulator region (57) of Hong having a thickness that allows tunneling of charge between the first and second floating gate (580) and the first channel region.

With respect to claims 59 and 61, the thickness of the first and second insulator region (57) of Hong is 100 Å (between 70 Å and 110 Å).

With respect to claims 62-65, the first and second vertical insulator (570) of Hong is made from a silicon dioxide or oxide nitride oxide (ONO) having a thickness that provides capacitance between the first and second floating gate (580) and the control gate (520), respectively, and the first and second vertical insulator (570) preventing leakage between the first and second floating gate (580) and the control gate (520), respectively.

With respect to claim 66, the first and second floating gate (580) of Hong each inherently being capable of storing multiple levels of charge.

With respect to claim 67, the first and second floating gate (580) of Hong each inherently being capable of storing four levels of charge.

With respect to claim 68, an oxide layer (57) of Hong is disposed on top of each diffusion region (59).

Response to Arguments

4. Applicant's arguments with respect to amended and new claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER